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United States Patent [19]

Devins et al.

[11] **Patent Number:** 5,784,595[45] **Date of Patent:** Jul. 21, 1998[54] **DMA EMULATION FOR NON-DMA CAPABLE INTERFACE CARDS**

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[51] **Int. Cl.⁶** G06F 31/00; G06F 13/32[52] **U.S. Cl.** 395/500; 395/821; 395/842;
 395/843; 395/846; 364/578[58] **Field of Search** 395/500, 821,
 395/842, 843, 846; 364/242.3, 242.31,
 242.34, DIG. 1, 578**References Cited****U.S. PATENT DOCUMENTS**

4,313,160 1/1982 Kaufman et al. 364/200
 4,658,350 4/1987 Eggebrecht et al. 364/200

4,665,481 5/1987 Stonier et al. 364/200
 4,665,482 5/1987 Murray, Jr. et al. 364/200
 4,751,634 6/1988 Burrus, Jr. et al. 364/200
 4,847,750 7/1989 Daniel 364/200
 5,088,033 2/1992 Binkley et al. 395/500
 5,274,779 12/1993 Stewart et al. 395/425
 5,381,538 1/1995 Amini et al. 395/483

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A method and system are disclosed for simulating a direct memory access (DMA) function to access memory in a host computer having a DMA controller for the purpose of enabling the transfer of data between the host memory and a computer accessory data handling device not capable of DMA operation. The accessory data handling device can be operably connected to the host. The address contents of the DMA controller can be read to determine the location in the host memory where data is to be transferred from the host memory to the accessory data handling device or from the accessory data handling device to the host memory. Data is read from the host memory at the address specified in the DMA controller and written to the accessory data handling device or read from the accessory data handling device and written to the host memory at the address specified by the DMA controller, respectively. The host computer is informed that a DMA operation corresponding to the data transfer has been completed when the data transfer required has been completed.

28 Claims, 4 Drawing Sheets